L Number	Hits	Search Text	DB	Time stamp
6	2084	transistor and (compound adj semiconductor)	USPAT; US-PGPUB	2002/04/16 16:40
7	84	(transistor and (compound adj semiconductor)) and spacers and nitride	USPAT; US-PGPUB	2002/04/16 16:40
8	12	((transistor and (compound adj semiconductor)) and spacers and nitride) and (refractory with metal)	USPAT; US-PGPUB	2002/04/16 16:40

L Number	Hits	Search Text	DB	Time stamp
1	4781	(nickel or Ni or ruthenium or Ru or vanadium or V or gold or Au or cobalt or Co) and (compound adj semiconductor)	USPAT; US-PGPUB	2002/04/16 12:40
2	2279	(nickel or Ni or ruthenium or Ru or vanadium or V or gold or Au or cobalt or Co) same (compound adj semiconductor)	USPAT; US-PGPUB	2002/04/16 13:04
3	2129	((nickel or Ni or ruthenium or Ru or vanadium or V or gold or Au or cobalt or Co) same (compound adj semiconductor)) and @ad<=20000928	USPAT; US-PGPUB	2002/04/16 12:41
4	132	(((nickel or Ni or ruthenium or Ru or vanadium or V or gold or Au or cobalt or Co) same (compound adj semiconductor)) and @ad<=20000928) and (HBT or (heterojunction adj bipolar adj transistor))	USPAT; US-PGPUB	2002/04/16 13:04
5	10	((((nickel or Ni or ruthenium or Ru or vanadium or V or gold or Au or cobalt or Co) same (compound adj semiconductor)) and @ad<=20000928) and (HBT or (heterojunction adj bipolar adj transistor))) and refractory	USPAT; US-PGPUB	2002/04/16 13:14
6	4509	(nickel or Ni or ruthenium or Ru or vanadium or V or gold or Au or cobalt or Co) same (compound adj semiconductor)	EPO; JPO; DERWENT; IBM_TDB	2002/04/16 13:04
8	0	(((nickel or Ni or ruthenium or Ru or vanadium or V or gold or Au or cobalt or Co) same (compound adj semiconductor)) and (HBT or (heterojunction adj bipolar adj transistor))) and refractory	EPO; JPO; DERWENT; IBM_TDB	2002/04/16 13:05
7	68	((nickel or Ni or ruthenium or Ru or vanadium or V or gold or Au or cobalt or Co) same (compound adj semiconductor)) and (HBT or (heterojunction adj bipolar adj transistor))	EPO; JPO; DERWENT; IBM_TDB	2002/04/16 13:05
9	122	((((nickel or Ni or ruthenium or Ru or vanadium or V or gold or Au or cobalt or Co) same (compound adj semiconductor)) and @ad<=20000928) and (HBT or (heterojunction adj bipolar adj transistor))) not (((((nickel or Ni or ruthenium or Ru or vanadium or V or gold or Au or cobalt or Co) same (compound adj semiconductor)) and @ad<=20000928) and (HBT or (heterojunction adj bipolar adj transistor))) and refractory)	USPAT; US-PGPUB	2002/04/16 13:14

DERWENT-ACC-NO: 1999-534804
DERWENT-WEEK: 200004

TITLE: Base electrode formation process for III-V group **heterojunction bipolar transistor** - involves performing heat treatment after forming base electrode which is laminated multilayer body, on group III-V semiconductor base layer and on palladium alloyed base layer

PATENT-ASSIGNEE: FUJITSU LTD[FUIT]

PRIORITY-DATA: 1998JP-0028037 (February 10, 1998)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 11233452 A	August 27, 1999	N/A	005	H01L 021/28

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP 11233452A	N/A	1998JP-0028037	February 10, 1998

INT-CL (IPC): H01L021/28; H01L021/331 ; H01L029/205 ; H01L029/73

ABSTRACTED-PUB-NO: JP 11233452A

BASIC-ABSTRACT: NOVELTY - Heat treatment process is done after forming a base electrode (11) on group III-**V compound semiconductor** base layer and on pd alloy group III-**V compound semiconductor** base layer. The base electrode is a multilayered laminated body which has pd layer, Ti layer, pt layer, Ti layer and **Au** layer in sequence.

USE - For III-V group **heterojunction bipolar transistor (HBT)** used in optical communication system.

ADVANTAGE - The high concentration impurity containing base layer is stable
after heat treatment. The electrode contact resistance is very low therefore
speed of operation is high.

DESCRIPTION OF DRAWING(S) - The figure shows the side sectional view of **HBT**.
(11) Base electrode.

CHOSEN-DRAWING: Dwg.2/2

TITLE-TERMS:
BASE ELECTRODE FORMATION PROCESS GROUP **HETEROJUNCTION BIPOLAR TRANSISTOR**
PERFORMANCE HEAT TREAT AFTER FORMING BASE ELECTRODE
LAMINATE MULTILAYER BODY
GROUP SEMICONDUCTOR BASE LAYER PALLADIUM ALLOY BASE LAYER

DERWENT-CLASS: L03 U11 U12

CPI-CODES: L04-A02; L04-E01A;

EPI-CODES: U11-C05F2; U12-D01A2; U12-E01A1;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C2000-010408
Non-CPI Secondary Accession Numbers: N2000-029863

DERWENT-ACC-NO: 1994-122114
DERWENT-WEEK: 199649

TITLE: **Heterojunction bipolar transistor** for e.g. gold air-bridge technology -
has mesa with gallium-arsenide layer serving as buffer layer between contact
layer on top of gallium-arsenide layer of thickness greater than 4000 Angstrom

INVENTOR: DELANEY, J B; FULLER, C R ; HENDERSON, T S ; MERCER, B S

PATENT-ASSIGNEE: TEXAS INSTR INC[TEXI]

PRIORITY-DATA: 1992US-0890887 (May 29, 1992) , 1994US-0255282 (June 7, 1994)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5569944 A	October 29, 1996	N/A	010	H01L 029/737
JP 06069227 A	March 11, 1994	N/A	012	H01L 021/331

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 5569944A	Cont of	1992US-0890887	May 29, 1992
US 5569944A	N/A	1994US-0255282	June 7, 1994
JP06069227A	N/A	1993JP-0125635	May 27, 1993

INT-CL (IPC): H01L021/331; H01L029/205 ; H01L029/73 ; H01L029/737
ABSTRACTED-PUB-NO: JP06069227A
EQUIVALENT-ABSTRACTS: US 5569944A

The **HBT** includes a **compound semiconductor** material structure comprising several
layers, a mesa, and a contact layer. At least one of the

structure layers is composed of e.g. GaAs (36), and one of the remaining layers (32) is formed of, e.g. AlGaAs. The mesa and the contact, e.g. **Au**, are on a layer of a third material which is doped a conductivity type opposite that of the GaAs and AlGaAs layers.

The mesa has a GaAs material layer atop an AlGaAs material layer, the GaAS layer serving as a buffer layer between a contact layer atop the original GaAs layer and the original AlGaAs layer. The original GaAs layer has a thickness greater than 4000 Angstrom and the original AlGaAs layer has a thickness less than that of the GaAs layer. The contact is adjacent the mesa.

USE/ADVANTAGE - For power transistor and low power logic transistor used in digital communications; SCR. Reference point for timing subsequent etches is established at point other than top of uppermost of layers, thereby improving accuracy with which depth of subsequent etching can be controlled. Improved etch depth accuracy directly relates to more producible and higher yield **HBT** devices. Permits mfr. of logic, transmitter, and receiver circuits on same chip.

CHOSEN-DRAWING: Dwg.1/13 Dwg.13/13

TITLE-TERMS:
HETEROJUNCTION BIPOLAR TRANSISTOR GOLD AIR BRIDGE TECHNOLOGY MESA GALLIUM ARSENIDE LAYER SERVE BUFFER LAYER CONTACT LAYER TOP GALLIUM ARSENIDE LAYER THICK GREATER ANGSTROM

ADDL-INDEXING-TERMS:
SILICON CONTROLLED RECTIFIER

DERWENT-CLASS: U11 U12

EPI-CODES: U11-C07C4A; U11-C18A2; U12-D01A2; U12-E01A1;
U12-E01B1;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1996-409431

DOCUMENT-IDENTIFIER: US 5523623 A
TITLE: Ohmic electrode for a p-type compound semiconductor and a bipolar
transistor incorporating the ohmic electrode

---------- KWIC ---------

ABPL:
An ohmic electrode for a p-type III-V compound semiconductor is disclosed. The
ohmic electrode formed on a p-type III-V compound semiconductor layer includes
nickel (Ni), titanium (Ti), and platinum (Pt) as main components in an
interface between the ohmic electrode and the p-type III-V compound
semiconductor layer.

BSPR:
The present invention relates to a low resistance ohmic electrode for
semiconductors composed of III--V group compounds having a p-type conductivity
(hereinafter, such a semiconductor will be referred to as a "p-type III-V
compound semiconductor"), and a bipolar transistor incorporating the ohmic
electrode. The present invention relates to a method for producing the ohmic
electrode end a method for producing the bipolar transistor.

BSPR:
The ohmic electrode for a p-type III-V compound semiconductor of the invention,
formed on a p-type III-V compound semiconductor layer, includes nickel (Ni),
titanium (Ti), and platinum (Pt) as main components in an interface between the
ohmic electrode and the p-type III-V compound semiconductor layer.

BSPR:

According to another aspect of the invention, a method for producing an ohmic
electrode for a p-type III-V compound semiconductor,
includes the steps of:
forming a metal layer including Ni, Pt, and Ti as main components on a p-type
III-V compound semiconductor layer directly or via a thin layer; and alloying
the metal layer with a portion of the p-type III-V compound semiconductor layer
by a heat treatment.

BSPR:
According to still another aspect of the invention, a bipolar transistor
includes: a semiconductor multilayer structure including at least on a p-type
III-V compound semiconductor layer; and a p-type ohmic electrode formed on the
p-type III-V compound semiconductor layer and including Ni, Ti, and Pt as main
components.

BSPR:
In one embodiment of the invention, the semiconductor multilayer structure
further includes at least on an n-type III-V compound semiconductor layer and
the bipolar transistor further comprises an n-type ohmic electrode formed on
the n-type III-V compound semiconductor layer and including gold (Au),
germanium (Ge), and Ni as main components.

BSPR:
According to still another aspect of the invention, a method for producing a
bipolar transistor includes the steps of: forming a first metal layer including
Ni, Pt, and Ti as main components on a p-type III-V compound semiconductor
layer directly or via a thin layer; and alloying the first metal layer with a
portion of the p-type III-V compound semiconductor layer by a heat treatment.

BSPR:
In another embodiment of the invention, the method further includes a step of
forming a second metal layer including **Au**, Ge, and **Ni** as main components on an
n-type III-**V compound semiconductor** layer directly or via another thin layer,
the step being conducted between the step of forming the first metal layer and
the alloying step.

BSPR:
In still another aspect of the invention, the second metal layer is
simultaneously alloyed with the n-type III-**V compound semiconductor** layer at
the alloying step.

BSPR:
According to still another aspect of the invention, a method for producing a
bipolar transistor includes the steps of: etching a part of a semiconductor
multilayer structure from the upper face thereof, wherein the semiconductor
multilayer structure includes a first n-type III-**V compound semiconductor**
layer, a p-type III-**V compound semiconductor** layer stacked above the first
n-type III-**V compound semiconductor** layer, and a second n-type III-**V compound**
semiconductor layer stacked above the p-type III-**V compound semiconductor**
layer, and etching is performed until the p-type III-**V compound semiconductor**
layer is exposed or until a thin layer remains on the p-type III-**V compound**
semiconductor layer; forming a first metal film on the exposed p-type
semiconductor layer or the exposed thin layer, the first metal film including
Ni, Ti, and Pt or Pd; simultaneously etching the first metal film and the
p-type III-**V compound semiconductor** layer until the first n-type III-**V compound**
semiconductor layer is exposed or until another thin layer

remains on the first
n-type III-V compound semiconductor layer; forming a second metal film on the
exposed first n-type III-V compound semiconductor layer or the exposed another
thin layer, the second metal film including Au, Ge, and Ni; and alloying the
first metal film with the p-type III-V compound semiconductor layer and
alloying the second metal film with the first n-type III-V compound
semiconductor layer by a heat treatment such that a p-type ohmic electrode and
an n-type ohmic electrode are simultaneously formed on the p-type III-V
compound semiconductor layer n-type III-V compound semiconductor layer,
respectively.

BSPR:
By forming a metal layer including Ni, Ti, and Pt on a p-type III-V compound
semiconductor layer directly or via a thin layer, and subjecting the metal
layer to a heat treatment, the Ni and Ti prevents the generation of high
resistance compounds such as PtAs.sub.2 or acts to prevent the Pt from becoming
diffused deeply into the p-type III-V compound semiconductor layer, thereby
providing a low contact resistance between the ohmic electrode and the p-type
semiconductor layer. Furthermore, an alloy composed of Ni, Ti, and Pt has a
lower Schottky junction with respect to p-type semiconductors than that
obtained in the case of Pt alone.

CLPR:
1. An ohmic electrode for a p-type III-V compound semiconductor, the ohmic
electrode being formed on a p-type III-V compound semiconductor layer, wherein
the ohmic electrode includes nickel (Ni), titanium (Ti), and one of platinum
(Pt) or palladium (Pal) as main components in an interface

between the ohmic
electrode and the p-type III-V compound semiconductor
layer.

CLPR:
2. The ohmic electrode for a p-type III-V compound
semiconductor according to
claim 1, wherein the ohmic electrode includes Pd.

CLPR:
3. The ohmic electrode for a p-type III-V compound
semiconductor according to
claim 1, wherein the ohmic electrode includes Pt.

CLPR:
4. The ohmic electrode for a p-type III-V compound
semiconductor according to
claim 1, wherein the ohmic electrode is prepared by forming
a metal layer made
of Ni, Ti, and one of Pt or Pd on the p-type III-V compound
semiconductor and
alloying the metal layer with a portion of the p-type III-V
compound
semiconductor through a heat treatment at a temperature in
a range of
360.degree. C. to 460.degree. C.

CLPR:
5. The ohmic electrode for a p-type III-V compound
semiconductor according to
claim 4, wherein the heat treatment is conducted at a
temperature in a range of
370.degree. C. to 420.degree. C.

CLPR:
6. The ohmic electrode for a p-type III-V compound
semiconductor according to
claim 4, wherein the metal layer comprises a multilayer
film comprising a Ni
layer, a Ti layer, and a Pt layer, the Pt layer being an
uppermost layer.

CLPR:
7. The ohmic electrode for a p-type III-V compound
semiconductor according to
claim 6, wherein the Ti layer has a thickness of 10 nm or

less.

CLPR:
8. A bipolar transistor comprising: a p-type III-V compound semiconductor layer; and an ohmic electrode formed on the p-type III-V compound semiconductor layer wherein the ohmic electrode comprises Ni, Ti, and one of Pt or Pd as main components.

CLPR:
9. The bipolar transistor according to claim 8 further comprising an n-type III-V compound semiconductor layer and a second ohmic electrode formed on the n-type 1II-V compound semiconductor layer wherein the second ohmic electrode comprises gold (Au), germanium (Ge), and nickel (Ni) as main components.

CLPR:
12. The bipolar transistor according to claim 8, wherein the ohmic electrode is prepared by forming a metal layer made of Ni, Ti, and one of Pt or Pd on the p-type III-V compound semicoductor and alloying the metal layer with a portion of the p-type III-V compound semiconductor through a heat treatment at a temperature of 370.degree. C. to 420.degree. C.